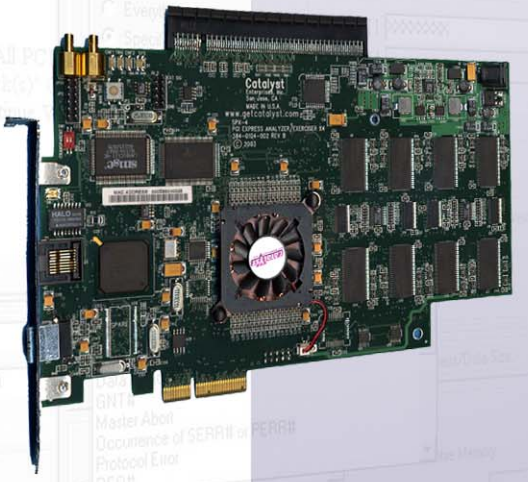
SPX SERIES

# PCI Express 開発ツール

**バス & プロトコルエキササイザ　SPX-1E,4E,8E,16E**
**バス & プロトコルアナライザ　SPX-1A,4A,8A,16A**
**PXP-100 開発プラットホーム**
**アナライザ/エキササイザバンドルSPX-1B,4B,8B,16B**

PCI EXPRESS



コンパクトサイズのアナライザ/エキササイザ
x1からx16 までのレーン数
非常に使いやすいGUI
SSC、低周波数クロック動作対応
アップ&ダウン ストリーム両方をリアルタイムで行うデバイスエミュレーション
ビットレベルの操作やエラー挿入を含む洗練されたトラフィック生成機能
強力なエキササイザのユーティリティ
強力トリガと取り込み時リアルタイムフィルタリング
コンプライアンステストスイート SpekChek
PXP-100とエキササイザで、マザーボード代わりに使用
ネットワークおよびUSB2.0をサポートしたホストインターフェース
取り込みデータをカットアンドペーストでエキササイザへ移行
ユーザサイトでのアップグレードFPGA design
ソフトウェアのアップデートはWebから無料でダウンロード可能

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PCI, PCI-X, USB, Bluetooth
PCI Express, SATA, SAS

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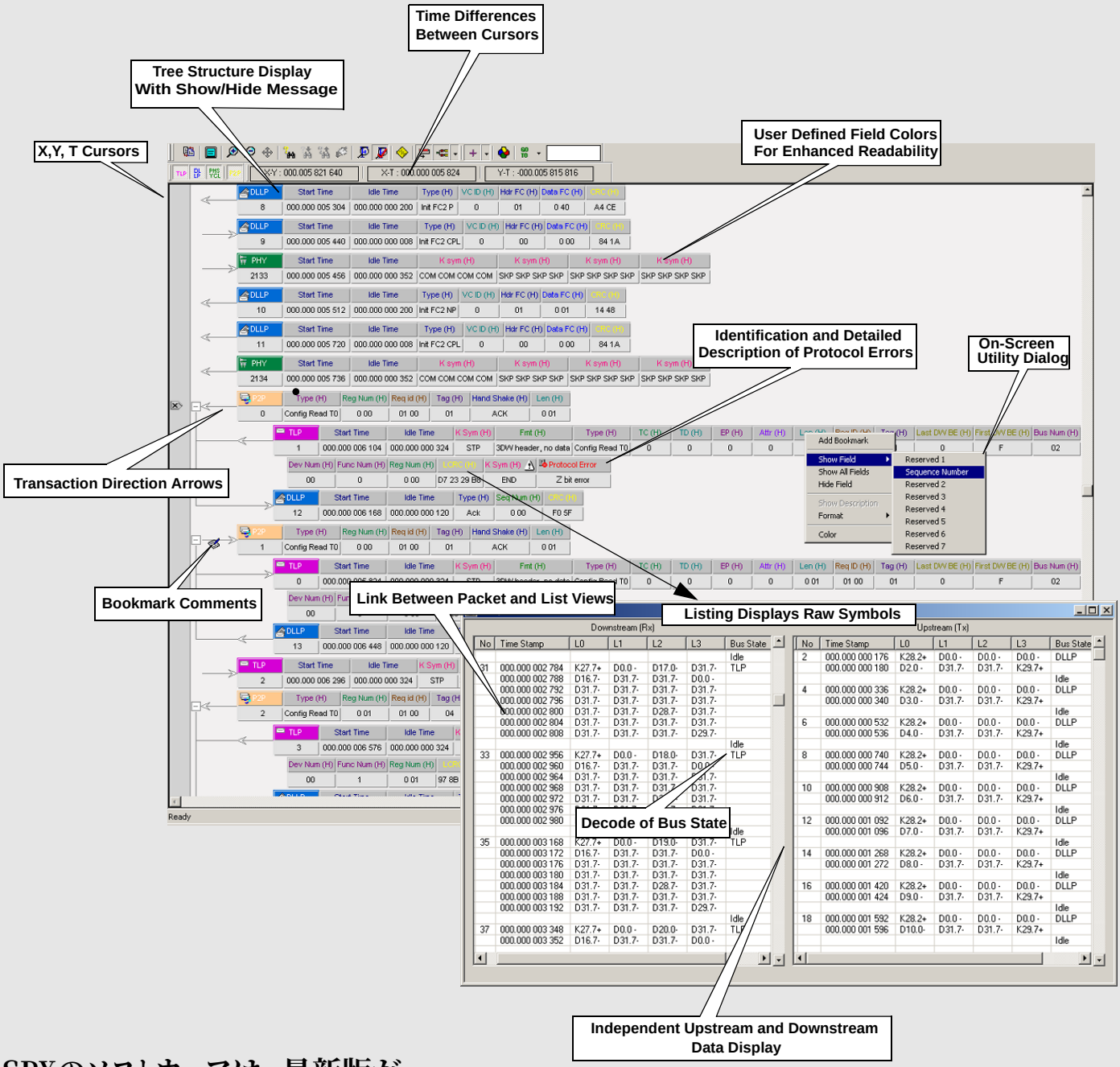
# SPX SERIES

## 見やすく、直観的に使いやすいソフトウェア




SPXのソフトウェアは、最新版が、
以下のアドレスでダウンロードできます。
http://www.getcatalyst.com/downloads.jsp

## PCI EXPRESS DEVELOPMENT TOOLS

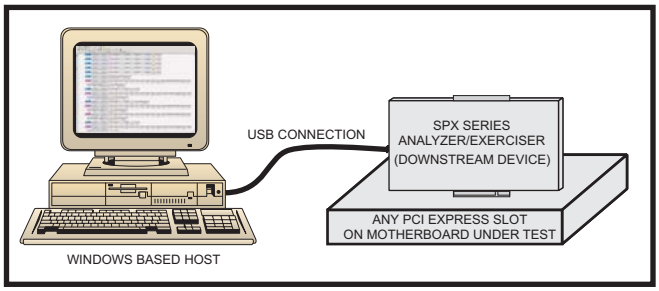
Catalyst Enterprises designs and manufactures a comprehensive set of powerful development solutions to aid PCI Express developers in achieving their design goals. This collection of tools includes:

- Bus & Protocol Exercisers
- Bus & Protocol Analyzers
- Development Platform
- Bus Extenders and Adapters

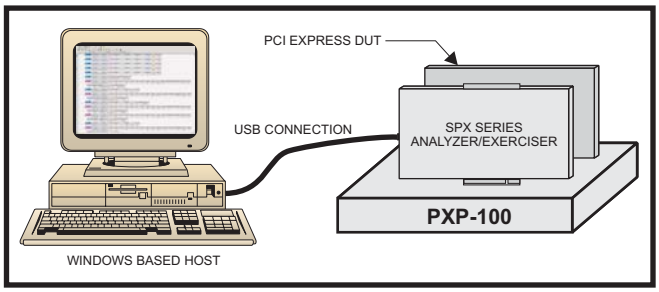
## VERSATILE EXERCISER

The SPX Series Exerciser offers the capability to transmit any form of PCI Express data across all protocol layers up to x16 lanes. Capable of emulating any Upstream or Downstream port, this tool can be utilized as a reference environment and a debugging aid for virtually any PCI Express component. The Exerciser interface offers extensive manipulation of various output parameters to give the user precise control over transmitted patterns. This characteristic makes the Exerciser an ideal tool starting with the early stages of product development through final design verification and compliance certification.

The Exerciser may be set to operate as an Endpoint (Downstream Device) or as a Platform (Upstream device) by user determined physical connection and corresponding Exerciser Settings selection.




**SPX Operating as an Endpoint**

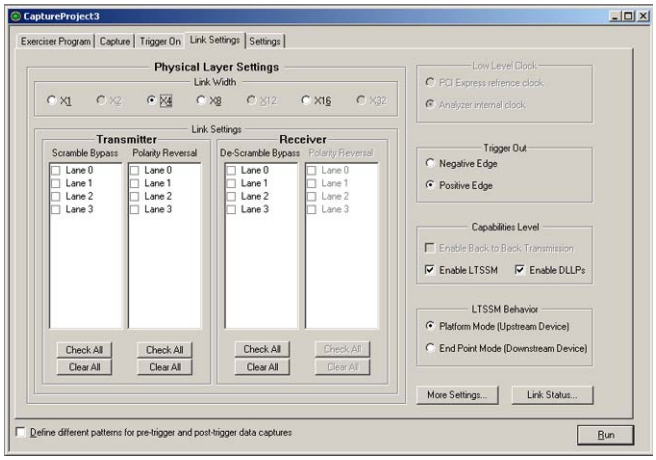



**SPX Operating as a Platform**

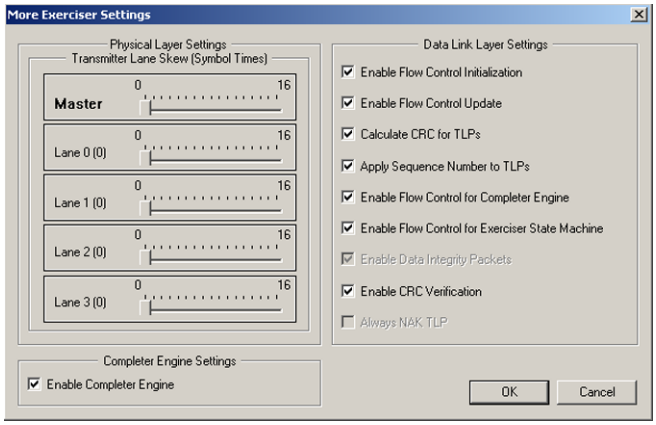
### EXERCISER MODES

Independently of operation as an Endpoint or Platform the Exerciser may be programmed at different levels of complexity.

For early stages of product development a **Pattern Generation** mode is offered requiring the user to program the interaction at Physical and Data Link layers. When operating in this mode, the Exerciser hardware disables the automatic logic for the Physical and Data Link Layers and outputs the commands at each layer exactly as composed by the user. For more advanced stages in development a **Real Mode** is offered. In this mode the majority of the Physical and Data Link Layer interchange is managed by the Exerciser hardware. The user is given the option to manipulate parameters of the Physical and Data links to a limited extent. This allows the user to focus on the Transaction Layer exclusively, yet is also permitted to manage the characteristics of the lower layers.



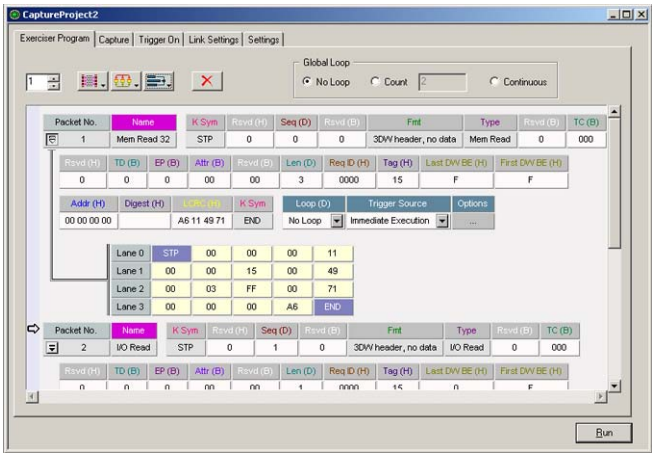

**Exerciser configuration options**



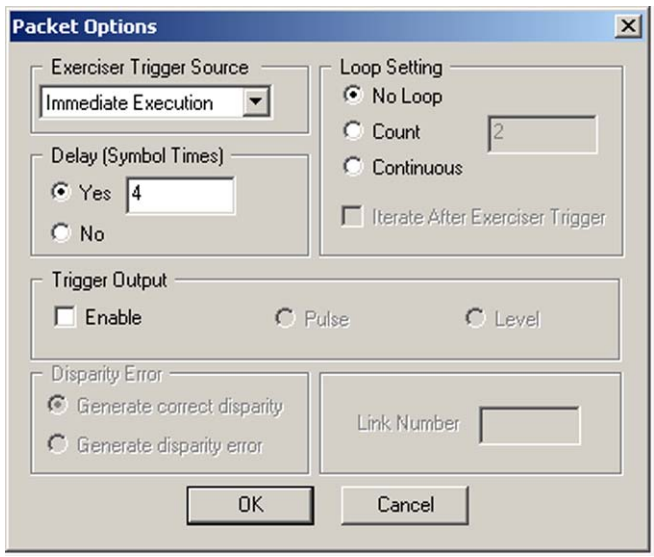

**Additional Exerciser settings**

## Advanced Mode Exerciser Program Features

The **Exerciser Program** is project based, streamlined graphical user interface for programming the Exerciser output data flow. Pre-defined commands, representing all PCI Express protocol elements, allow rapid construction of test scenarios with a minimum of effort. In **Real Mode**, defining a higher layer command sequence automatically defines the required lower layer support. Sample projects are provided with the SPX software to reduce user setup effort to quickly apply test stimulus and analyze behavior such as response to errors and stress testing. These projects are also useful as templates to create customized tasks.




**Exerciser Program command entry with Symbol Expansion**




**Individual command settings**

Programming features:

- Generation of any TLP, DLLP, Ordered Set commands in Real or Pattern Generation modes
- Modification of all fields in any command
- Simultaneous support of all protocol layers within any command sequence
- Automatic calculation of LCRC, ECRC, Digest, TLP Sequence Number values
- **Symbol Expansion** for raw manipulation of individual symbol values per each lane
- **Exerciser Trigger** for pacing transmission of each command
- Cursors
- Bookmarks

## Looping

A two level nested program loop capability allows the user to develop complex command sequences that adapt to changing responses. The user may set the exerciser to:

- Loop the entire traffic sequence up to 64 thousand times, or infinitely
- Loop any individual packet up to 4096 times, or infinitely
- Control each iteration of packet loop execution with **Exerciser Trigger**
- **Trigger Output** to signal an external device upon occurrence of command transmission

## Error Injection

The SPX Exerciser offers multiple ways to introduce intentional anomalies and errors in the generated traffic stream. Error injection allows the user to recreate receiver errors, malformed TLPs, transaction ordering rule violations, corner case scenarios and numerous other test conditions. The user friendly **Exerciser Program** GUI allows:

- User-Defined commands to create irregular packets
- Undefined and Reserved encoding for packet fields
- **Back-to-back** packet execution and bypass of internal buffering for bus utilization stress testing†
- Control of Physical Layer , per each lane
  - Scrambling/De-Scrambling Bypass
  - Polarity Inversion
  - Lane Delay (Lane-to-Lane Skew)
  - Running Disparity error generation†
  - Substitution of Data or Special Symbols in any location
- Delayed command transmission
- Control of Data Link Layer
  - Flow Control Initialization and Updates
  - Manipulation of Flow Control Credit values†
  - Bypass Flow Control Tracking
  - Automatic or User defined CRC value
  - Automatic or User defined Sequence number
  - Disable ACK/NAK
  - Always NAK TLPs

## Real Device/Pattern Generation

Integrated PCI Express intelligence allows the Exerciser to participate as an active agent in a PCI Express system. This capability may be disabled to make the SPX a pattern generator. As an Agent the Exerciser offers the following capabilities:

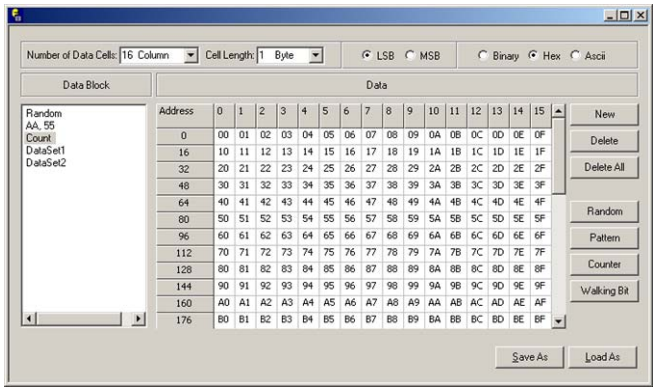
- Fully programmable Configuration Space†
- Local Memory to allow random access read/write operation to the Exerciser†

## Data Blocks

Payload data for commands may be created as **Data Blocks** by using a convenient GUI or imported from other sources. Data blocks may be created with the following types of data patterns:

- Random
- Repetitive
- Incrementing/decrementing counter
- Walking 0 or 1

Data may be imported from or exported to other sources in binary or text formats.




**Data blocks for data payload**

## Memory Test Suite†

This set of Exerciser utilities performs memory access verification operations on user-specified address range using SPX COM API to:

- Perform a memory dump from an address range
- Read memory contents, modify and write new value, and read back to verify operation
- Read memory contents, modify and write new value
- Read and write to a specified address
- Scan configuration spaces of downstream components on local and any subordinate links

## Cross Triggering

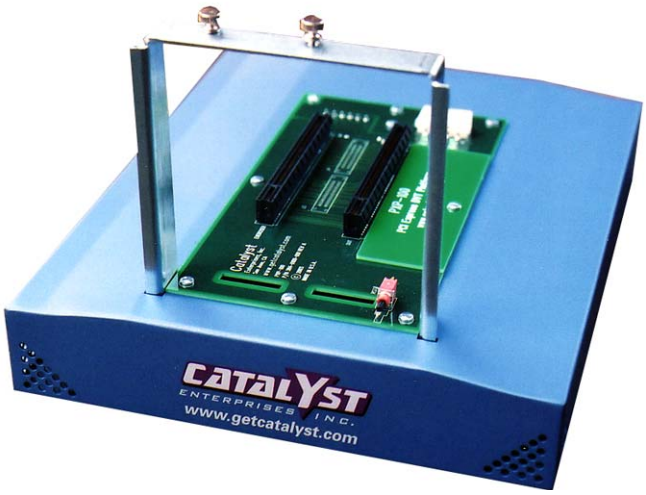
The SPX Exerciser integrates the interface to enable cross triggering with external devices. An External Trigger output from the Exerciser signals an external device on the occurrence of a Command transmission. An External Trigger input (output from an external device) tags the command transmission from the Exerciser. External Triggers may be configured for polarity.

## Integrated Capture

If the SPX Exerciser option is enabled alone, it incorporates a scaled down set of analyzer capture and trigger functions. To perform a full function capture and trigger the analyzer option must be enabled.

## PXP-100 DVT PLATFORM

The PXP-100 PCI Express development platform complements the Exerciser in Platform mode and eliminates the requirement for a motherboard to connect to a card under test. The PXP-100 is a passive backplane designed to connect the SPX Exerciser as a Platform (upstream device) to the Card Under Test.

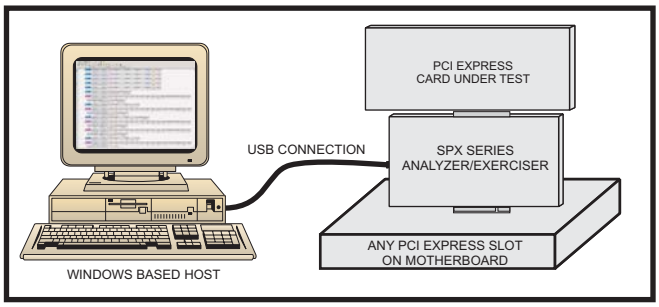



### THE PXP-100 FEATURES:

- Self-contained, portable, and self powered
- Supplies power for +3.3V, +3.3Vaux, and +12V rails, as well as a power source for SPX
- Generates PCI Express Reference Clock
- Generates valid PERST# bus reset that can be activated by a manual push button.
- Mid-bus probe pads for connection to bus monitoring equipment
- Two x16 slot connectors accept various combinations of cards of any link width

## HIGH PERFORMANCE ANALYZER

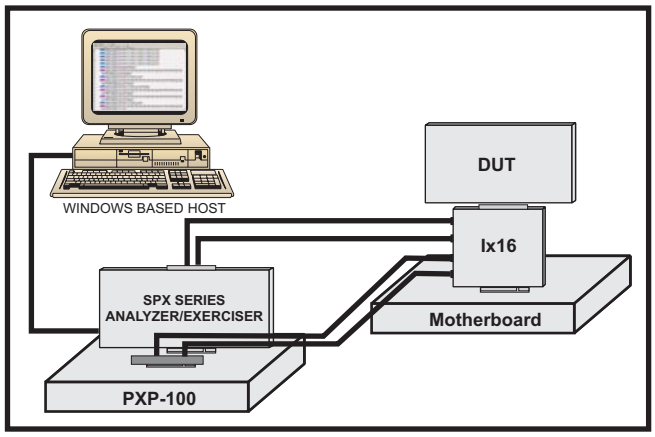
The SPX Series Analyzer is a PCI Express serial bus analyzer that is designed to be the optimal bus analysis tool for a wide range of applications in an up to x16 environment. A powerful, reconfigurable hardware engine enables flexible capture and trigger of Transaction and Data Link Layer Packets, Physical Layer Ordered Sets and all bus conditions while maintaining an easy-to-use interface. SPX Series software natively supports multiple analyzers within the same application for enhanced analysis of multiple nodes within the PCI Express hierarchy.




**SPX Analyzer connection**

The SPX Analyzer is introduced between any PCI Express slot on the motherboard and the Card Under Test permitting simultaneous analysis in both directions of information flow. The SPX Analyzer operates with minimum intrusion using ultra high speed analog buffers that eliminate the need for extra cabling. An External power source eliminates the need for the SPX to use power from the mother board in order to debug system power up problems.

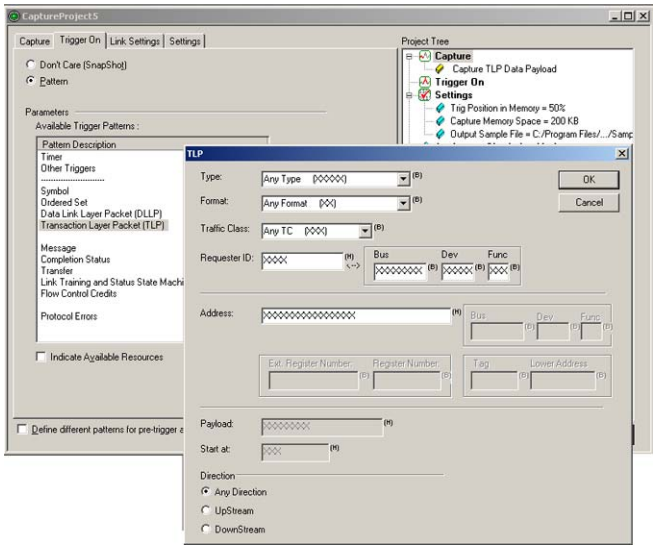
As an alternate probing method, the IX16 passive interposer card may be used between the motherboard and the DUT.




**Analysis using Passive Interposer**

### EASY MODE DATA CAPTURE & TRIGGER

This interface allows hardware or software oriented PCI Express debug without requiring complex programming or special setup of the Analyzer. A comprehensive selection of pre-defined setups is made available for immediate analysis of most commonly encountered scenarios. A convenient Project Tree display shows a comprehensive of selected capture and trigger choices.

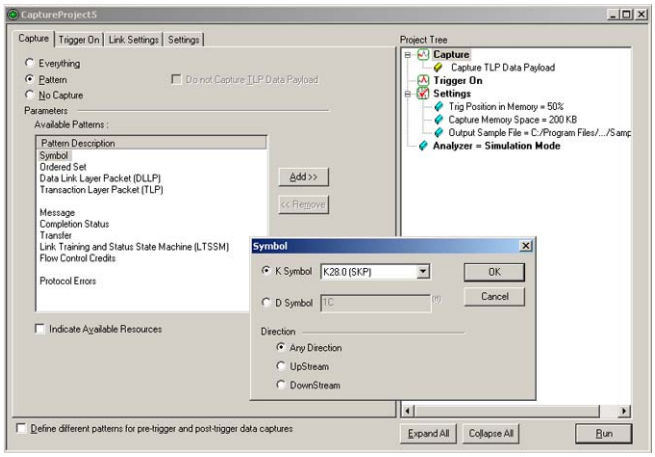



**TLP filter/trigger settings**

### REAL TIME FILTER SELECTIONS

The following selections are available pre-defined capture categories:

- Everything – Do not filter
- Exclude DLLPs – quick exclude
- Exclude Idle - quick exclude†
- Exclude Upstream Traffic - quick exclude†
- Exclude Downstream Traffic - quick exclude†
- Exclude Ordered Sets – quick exclude
- Exclude TLP Data Payload – quick exclude†
- Symbols – D or K
- Ordered Sets
- DLLP
- TLP
- Messages
- Completion Status
- LTSSM States
- Flow Control Credits
- Protocol Errors - Enables display of protocol errors




**Symbol filter/trigger settings**

For more specific data capture, the patterns can have additional parameters applied. Up to 3 capture patterns from each category can be specified for Upstream, Downstream or either direction.

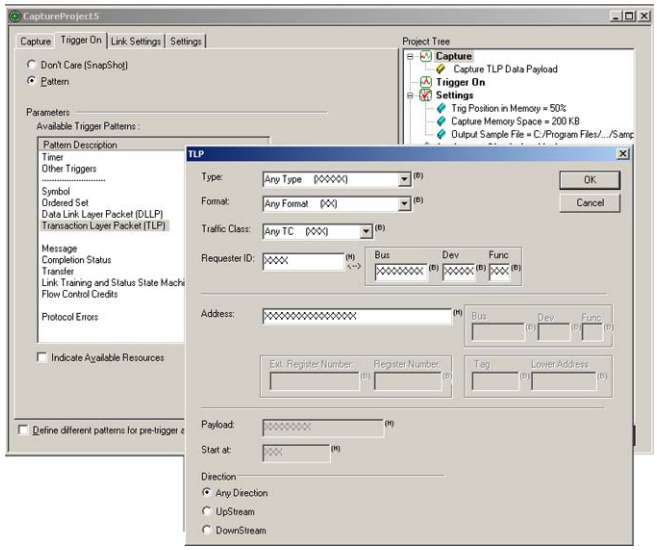
## Partitioned Data Capture

The SPX series analyzer capture settings may be set to one set of capture patterns prior to the occurrence of a trigger and to a different set of for capture after the occurrence of a trigger.

## Extensive Triggering

The SPX Series analyzer offers the following pre-defined trigger categories:

- Snapshot – Trigger immediately
- Timer – Trigger after timer expiration
- External Input – Synchronization with other equipment or any external event
- Wake# - Trigger on transition of Wake# signal
- Symbols
- Ordered Sets
- Data Link Layer Packet
- Transaction Link Layer Packet
- Messages
- Completion Status
- LTSSM States
- Flow Control Credits by Traffic Class
- Protocol Errors – Trigger on all or any selected protocol errors




**TLP trigger setting**

Each of the triggering categories may be further refined for more specialized triggering. Up to 3 triggering patterns in any category can be specified for Upstream, Downstream or either direction. A **Sequential Trigger** allows the listed trigger selections to be arranged in a user defined order to define a triggering sequence, or be set to trigger on the occurrence of any selection.

## Protocol Error Checker

SPX Series Analyzer hardware monitors, detects and can trigger on different protocol errors in real-time. Additional Protocol Errors are detected by post-capture processing for an extensive error analysis at all layers.

### Real-Time Protocol Errors

- ECRC Error
- DLLP CRC Error
- LCRC Error
- Invalid Symbol Encoding
- Running Disparity Error
- Additional Protocol Errors in future releases

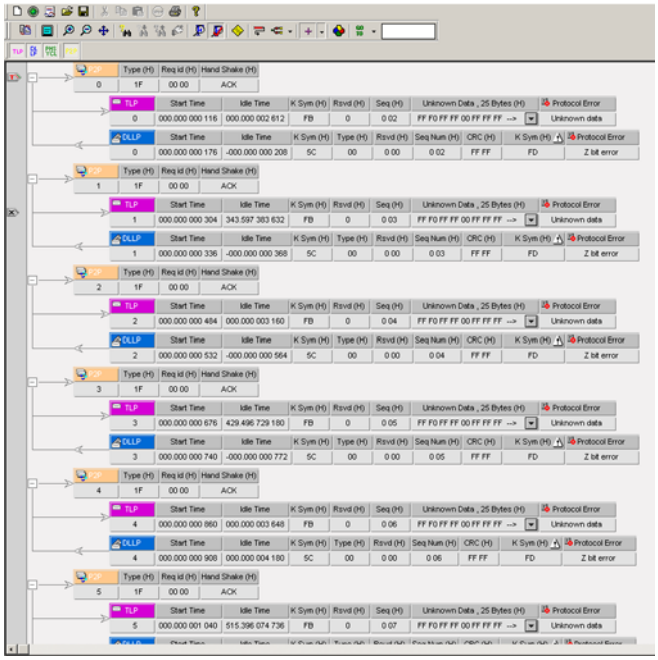
## Deep Capture Buffer

A high capacity capture buffer up to 1GB (Optional) allows for the capture of data over long periods of bus activity. Coupled with the advanced triggering and filtering capability this allows easy debugging of intermittent problems.

# DISPLAY CAPABILITY

The Ultimate Graphical User Interface display offers a significant set of features to assist in analyzing captured data. Multi-layer viewer show/hide modes are useful to view traffic for the layer of interest only.

## PACKET VIEW

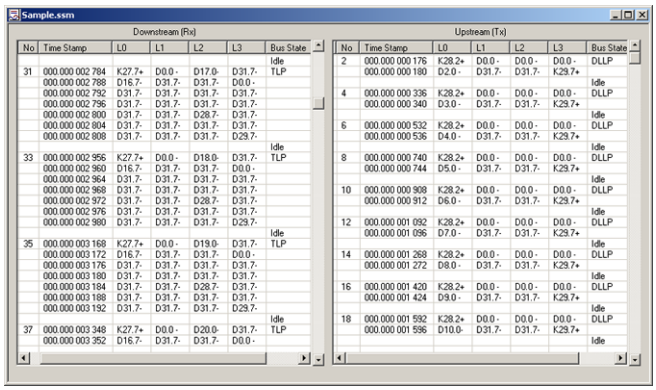


**Decoded packet view**

The results window provides for:

- Display of all Transactions, Packets, and bus conditions
- Grouping of related packets by **Point-to-Point** (across link) and **End-to-End** (across hierarchy)
- Decoding of Packet Fields and Special Symbol names
- Packet Wrapping to eliminate horizontal display scrolling
- Crosslink between Viewer modes
- Identification and description of detected Protocol Errors
- **Smart On-Screen** filtering of Transaction, Data Link, Physical Layers and utility access
- Export in Text Format
- Format of data in Hexadecimal, Binary, or ASCII
- Notes and Bookmarks
- Time calculation services including Packet Start Time, Bus Idle Time, and time between X, Y, Trigger Cursors
- Go to X, Y, Trigger Cursors and Packet Number

## LIST VIEW




**Symbol listing view**

The results window provides for

- Raw symbol dump of captured data organized according to link width
- Recognition of packets and state of bus
- Split windows for Upstream & Downstream traffic
- Format of data in Hex, Binary, 10B with disparity
- Identification of protocol errors
- Cursors

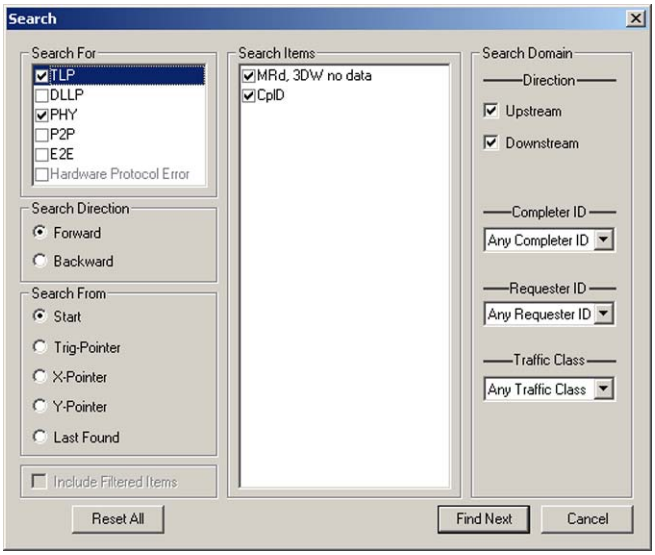
## POST PROCESSING DISPLAY SERVICES

The SPX Series incorporates efficient software algorithms to provide for expedient results for Search and Filtering of the data regardless of selected capture buffer size.

### SEARCH UTILITY

The Packet View search utility offers you the capability to:

- Search for packets in Transaction Layers by any packet field
- Search for TLP payload data†
- Search for packets in Data Link Layers
- Search for ordered sets in Physical Layers
- Search the above in Upstream, Downstream, or both directions
- Search from start, end, X, Y or Trigger cursors in the viewer




**Search utility**

### PACKET VIEWER FILTERING

The filter may be used to exclude unwanted items from the display. The filter selects for exclusion/inclusion of :

- Quick Filter of Transaction, Data Link, Physical Layers
- Specific packets in Transaction Layer by Requester/ Completer ID
- Specific packets in Data Link Layer
- Specific packets by Traffic Class
- Specific packets with Protocol Errors

### STATISTICAL ANALYSIS

#### REAL-TIME STATISTICS

- Real time graphical display of Statistics for:
  - Throughput measurement
  - Link usage measurement
  - Payload measurement
  - Latency

#### STATISTICAL REPORT

- Analysis of captured data.
- Summary of capture packets
- Summary of bus throughput, utilization, and other performance parameters

### UTILITIES

#### BUS VOLTAGE CHECKS†

SPX monitors the condition of +3.3V, +12V, and +3.3VAux system power rails and reports when voltage falls below valid levels.

## COM API

The SPX Series software includes a set of interfaces that add scripting or automation capabilities to the Analyzer and/or Exerciser. This may be used to create custom applications for a specific testing task using any programming package that supports the Common Object Model. The API library allows direct access to most of the Analyzer/Exerciser functions to manipulate project output files and hardware settings without the need of the Analyzer/Exerciser GUI. These capabilities allow the Analyzer/Exerciser to become a production level tester or compliance verification tool. The COM API offers:

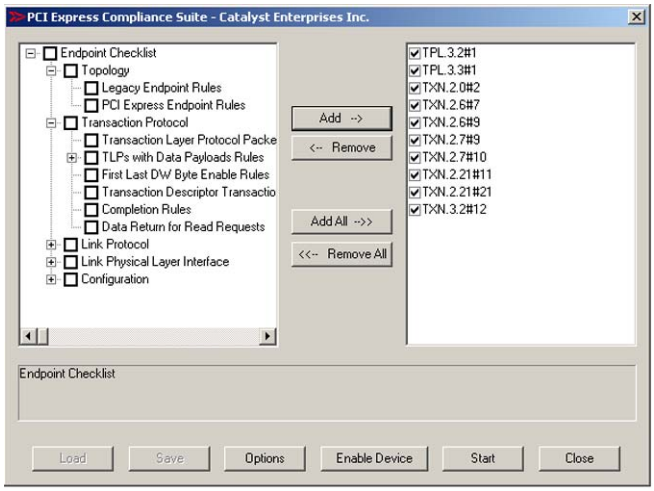
- High Level **Easy Mode** programming
- Detail Level **Advanced Mode** programming
- Support by development platforms such as Microsoft Visual C++, Microsoft Visual Basic, Borland Delphi
- Export of all project settings and utilities available in the GUI
- XML formatted Project files for text-based manipulation

## COMPLIANCE TESTING

The SPX incorporates a GUI based “Compliance Test Suite” that performs tests from the following 5 **PSIG Compliance Specification Check Lists**:

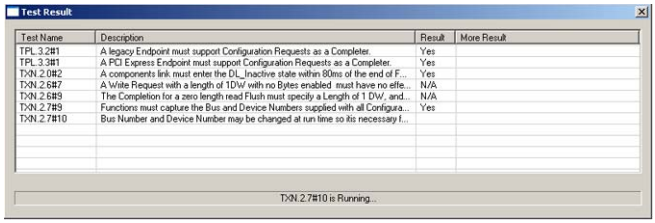
- Endpoint Topology
- Endpoint Transaction Protocol
- Endpoint Link Protocol
- Endpoint Link - Physical Layer Interface
- Endpoint Configuration

The user may select any or all of the tests from each list using a GUI based Test Selection dialog.




**Test Selection Dialog**

The Test Output is a Pass/Fail display with a corresponding test description.

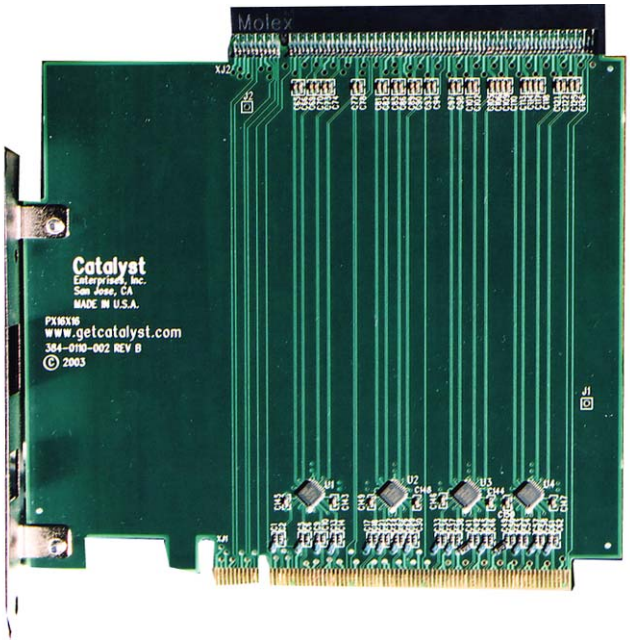



**Test Result Display**

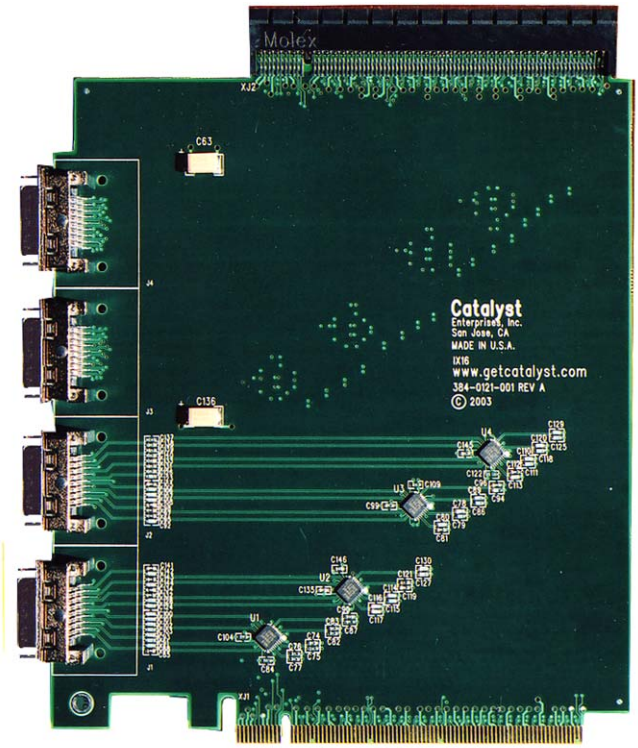
For more detail see the **SPX Endpoint Compliance Data Sheet**.

## PCI EXPRESS ADAPTERS/EXTENDERS

Catalyst Enterprises offers an extensive line of PCI Express extenders and adapters to function as bus and width configuration converters, and to ease access to card connections in a lab environment. All products are carefully designed to minimize signal distortion.




**PEX16216**




**IX16**

### PCI EXPRESS X16 TO X16 ACTIVE EXTENDER

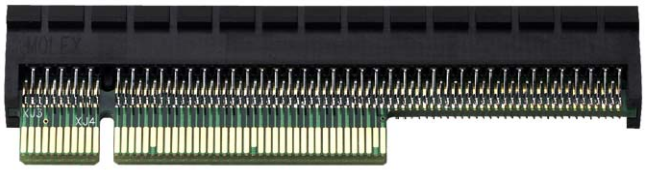
**PEX16216** is an active bus riser enabling a 4.5”(11.4 cm) extension to x16 slots. It uses ultra-high speed analog buffers.

### PCI EXPRESS X16 PASSIVE EXTENDER

**IX16** is a passive interposer with a high impedance active probe.

## PCI Express x16 to x8 Adapter

**PEA1628** is a passive bus width conversion adapter enabling a down-plug connection of x16 card into a x8 slot.

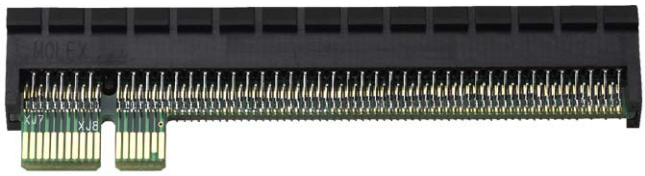


## PCI Express x16 to x4 Adapter

**PEA1624** is a passive bus width conversion adapter enabling a down-plug connection of x16 or x8 card into a x4 slot.

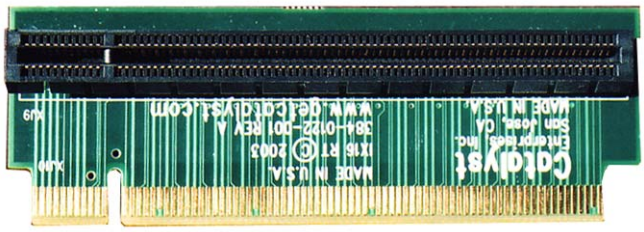
## PCI Express x16 to x1 Adapter

**PEA1621** is a passive bus width conversion adapter enabling a down-plug connection of up to x16 card into a x1 slot.



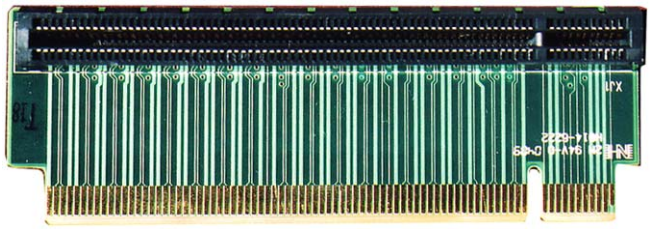
## PCI Express x16 Right Angle Adapter, A side up

**PEART16A** is a passive bus adapter enabling the user to rotate the card 90 degrees allowing A side probing.



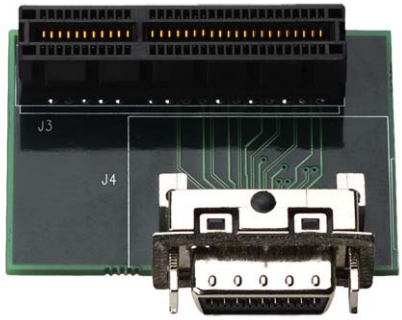
## PCI Express x16 Right Angle Adapter, B side up

**PEART16B** is a passive bus adapter enabling the user to rotate the card 90 degrees allowing B side probing.



## Infiniband x4 to PCI Express x4 Adapter

**IB2X4** is a passive bus conversion adapter between Infiniband and PCI Express in a x4 lane width configuration.



## ORDERING INFORMATION

The SPX Series features a flexible, field upgradable FPGA-based engine with free lifetime software updates for the product including enhancements to the product as purchased.

**Note:** Catalyst Enterprises, Inc. reserves the right to appoint any product enhancement as a separate purchasable option. Additional options may be purchased at a later time following your initial order.

| Part# | ANALYZERS & EXERCISERS |
|---|---|
| SPX-1A | PCI Express x1 Bus & Protocol Analyzer |
| SPX-1E | PCI Express x1 Exerciser with Data Capture |
| SPX-1B | PCI Express x1 Analyzer & Exerciser Bundle |
| | |
| SPX-4A | PCI Express x4 Bus & Protocol Analyzer |
| SPX-4E | PCI Express x4 Exerciser with Data Capture |
| SPX-4B | PCI Express x4 Analyzer & Exerciser Bundle |
| | |
| SPX-8A | PCI Express x8 Bus & Protocol Analyzer |
| SPX-8E | PCI Express x8 Exerciser with Data Capture |
| SPX-8B | PCI Express x8 Analyzer & Exerciser Bundle |
| | |
| SPX-16A | PCI Express x16 Bus & Protocol Analyzer |
| SPX-16E | PCI Express x16 Exerciser with Data Capture |
| SPX-16B | PCI Express x16 Analyzer & Exerciser Bundle |

| Part# | ADAPTERS, MIDBUS, EXTENDERS AND DEVELOPMENT PLATFORM |
|---|---|
| **Adapters** | |
| PEA1621 | PCI Express x16 to x1 Adapter |
| PEA1624 | PCI Express x16 to x4 Adapter |
| PEA1628 | PCI Express x16 to x8 Adapter |
| IB2X4 | Infiniband x4 to PCI Express x4 |
| PETERMX | PCI Express x16, 50 ohm Bus Terminator Adapter |
| PELOOP-BACK | PCI Express Loop Back Adapter. Tx to Rx Bus for Link Training Verification |
| PEART16A | PCI Express X16 Right Angle Adapter A Side up |
| PEART16B | PCI Express X16 Right Angle Adapter B Side up |
| | **Prices reflect premium price paid for parts and are subject to change when part prices reduce.* |
| **MidBus** | |
| PEMID-BUS-8 | Kit for MidBus Probing Interface. Includes Mid-Bus Probe Interface, Cables, Analyzer Interface and 5 sets of hardware for securing probe to the board under test. Includes PCI Express Two x16 slot, self contained, self powered Development Platform with Clock & Reset Generation Circuitry |
| **Extenders** | |
| PEX16216 | PCI Express x16 To x16 Active Extender. PEX16216 is an active bus riser enabling a 4.5” (11.4 cm) extension to x16 slots |
| IX16 | PCI Express x16 Passive Extender/Interposer Probe |
| **Development Platform** | |
| PXP-100 | PCI Express Two x16 slot, self contained, self powered Development Platform with Clock & Reset Generation Circuitry |
| **Bundle** | |
| PE-DVT-B | Development Kit Bundle includes PXP-100, PEA1621, PEA1624, PEA1628, PETERMX, PELOOP-BACK and PEX16216 |

# SPECIFICATIONS

## SPX SPECIFICATIONS

### PCI EXPRESS PROTOCOL SUPPORT

| | |
|---|---|
| Specification Compliance | Revision 1.0a |
| Signaling Rate | Generation 1 (2.5Gb/s) |
| Physical Link Configuration | (x4) x4 Physical - x1, x2†, x4 Logical<br>(x16) x16 Physical - x1, x2†, x4, x8, x12†, x16 Logical |
| Supported Form Factors | Add-In Card |
| Virtual Channel Support | Analyzer - Channels 0 - 7<br>Exerciser - Channel 0 |
| Reference Clock | On-board precision clock or PCI Express slot reference clock, Spread Spectrum Clocking supported |
| Power Management | Not supported presently |
| Hot-Plug/Hot Swap | Not supported presently |

### ANALYZER

#### PROBE CHARACTERISTICS

| | |
|---|---|
| Probe type | Active Ultra High Speed analog buffers |
| Symbol Lock Time | ≈ 7µsec |

#### GENERAL

| | |
|---|---|
| Capture Buffer Size | (x4) 512MB (256MSym)<br>1GB (512MSym) |
| Capture Size | 1KB – 1GB, 1 KB increment |
| Analyzer Trigger Sources | Real-time Event Based Manual<br>External trigger input<br>Wake# signal |
| Time-Tag Recording Resolution | 4 ns |
| Time-Tag Width | 40 bits |
| Time-Tag Max Recording Duration | Approx. 1¼ hours |

### EXERCISER

| | |
|---|---|
| Exerciser Program Memory | (x4) 2MB<br>(x16) 8MB |
| Exerciser Local Memory | 1MB |
| Exerciser Capture Buffer | (x4) 2MB<br>(x16) 8MB |
| Program Looping Strategies | Global Loop<br>Per-packet loop, two level nesting |
| Program Global Loop | None or 2 – 65535 iterations |
| Per-packet loop | None or 2 – 4095 iterations |
| Packet output execution (Exerciser Trigger) | Immediate<br>Analyzer trigger<br>Manual software button<br>External Input |
| Packet Execution Delay | None or 4 Sym – 16MSym Times |
| Interpacket Delay | Back-to-Back – 3 Sym Times max.<br>Normal – 15 Sym Times max. |
| Outstanding Requests supported | TBD |
| Retry Buffer | TBD |
| Max Data Payload Support | 4KB per packet |

### EXTERNAL I/O

| | |
|---|---|
| External Trigger Input | 1 input, programmable as positive or negative |
| External Trigger Output | 1 output, programmable as positive or negative level or pulse |
| Signal Interface Levels | Standard LVCMOS |

### SYSTEM VOLTAGE CHECKS

| | |
|---|---|
| Power rails monitored | +3.3V, +12V, +3.3VAux, External Supply |
| Drop measured | -9% for +3.3V, +3.3VAux<br>-8% for +12V<br>-5% for External Supply |

### HOST SYSTEM CONNECTIONS

| | |
|---|---|
| Interfaces | USB 2.0 (High & Full Speeds)<br>10/100 Ethernet |

### PHYSICAL

#### PHYSICAL CHARACTERISTICS

| | |
|---|---|
| Dimensions | (x4) 8.4”(21.3 cm) W x 5.9” (15 cm) H<br>(x16) 7.4”(18.8 cm) W x 5.9” (15 cm) H |
| Operating Temperature | 40 - 85°F (5 – 30°C) |

### CONNECTIONS

| | |
|---|---|
| Top PCI Express connection | (x4) x16 standard slot connector |
| Bottom PCI Express connection | (x4) x4 standard edge card connector<br>(x16) x16 standard edge card connector |

| | |
|---|---|
| Ethernet Port | RJ45 |
| USB Port | USB type Standard-B |
| Power Supply | Bus slot +12V or External |

**Note1: Specifications subject to change without notice.**
**Note2: Items marked with † currently not implemented.**

### POWER SUPPLY

| | |
|---|---|
| Power Requirements | (x4) +12V, 2A Max<br>(x16) +12V, 5A |
| Power Consumption | (x4) 20W Typ.<br>(x16) 55W Typ. |

### STATUS LEDS

Analyzer Trigger
Board Configured
Voltage Checks Good/Fail (SYS)
Ethernet Port Status

### BUTTONS

Board Reset

### SYSTEM REQUIREMENTS

| | |
|---|---|
| Processor | Intel Pentium III 500MHz, or equivalent |
| Memory | 128MB |
| Display | 1024x768 resolution, 16 bit color |
| Operating System | Windows NT 4.0 SP6, Windows 98/98SE, Windows ME, Windows 2000, Windows XP |
| Hard Drive | 100MB space on partition with SPX software, 10MB space on Windows partition. |

### PXP-100 SPECIFICATIONS

| | |
|---|---|
| Reference Clock | 100MHz, unmodulated |
| Slot Connections | Two x16 standard connectors |
| Mid-bus probe pads | Two x8, bi-directional |
| Supplied Voltage Rails | +3.3V & +3.3VAux, 7A<br>+12V, 3A |

### PHYSICAL

#### PHYSICAL CHARACTERISTICS

| | |
|---|---|
| Dimensions | 10.5” (26.67cm) L x 8.7” (22.1cm) W x 6.5” (16.5cm) H |
| Operating Temperature | 40 - 85°F (5 – 30°C) |

### POWER SUPPLY

| | |
|---|---|
| AC Power | (100-120)VAC/<br>(200-240)VAC , 47-63Hz |

**PXP-100 Midbus Connector Pin Assignment**

| J3 Lanes 0 - 7 | | | | J4 Lanes 8 - 15 | | | |
|---|---|---|---|---|---|---|---|
| **PAD#** | **Signal** | **Pads#** | **Signal** | **PAD#** | **Signal** | **Pads#** | **Signal** |
| 2 | GND | 1 | Lane0 Tx+ | 2 | GND | 1 | Lane8 Tx+ |
| 4 | Lane0 Rx+ | 3 | Lane0 Tx- | 4 | Lane8 Rx+ | 3 | Lane8 Tx- |
| 6 | Lane0 Rx- | 5 | GND | 6 | Lane8 Rx- | 5 | GND |
| 8 | GND | 7 | Lane1 Tx+ | 8 | GND | 7 | Lane9 Tx+ |
| 10 | Lane1 Rx+ | 9 | Lane1 Tx- | 10 | Lane9 Rx+ | 9 | Lane9 Tx- |
| 12 | Lane1 Rx- | 11 | GND | 12 | Lane9 Rx- | 11 | GND |
| 14 | GND | 13 | Lane2 Tx+ | 14 | GND | 13 | Lane10 Tx+ |
| 16 | Lane2 Rx+ | 15 | Lane2 Tx- | 16 | Lane10 Rx+ | 15 | Lane10 Tx- |
| 18 | Lane2 Rx- | 17 | GND | 18 | Lane10 Rx- | 17 | GND |
| 20 | GND | 19 | Lane3 Tx+ | 20 | GND | 19 | Lane11 Tx+ |
| 22 | Lane3 Rx+ | 21 | Lane3 Tx- | 22 | Lane11 Rx+ | 21 | Lane11 Tx- |
| 24 | Lane3 Rx- | 23 | GND | 24 | Lane11 Rx- | 23 | GND |
| 26 | GND | 25 | Lane4 Tx+ | 26 | GND | 25 | Lane12 Tx+ |
| 28 | Lane4 Rx+ | 27 | Lane4 Tx- | 28 | Lane12 Rx+ | 27 | Lane12 Tx- |
| 30 | Lane4 Rx- | 29 | GND | 30 | Lane12 Rx- | 29 | GND |
| 32 | GND | 31 | Lane5 Tx+ | 32 | GND | 31 | Lane13 Tx+ |
| 34 | Lane5 Rx+ | 33 | Lane5 Tx- | 34 | Lane13 Rx+ | 33 | Lane13 Tx- |
| 36 | Lane5 Rx- | 35 | GND | 36 | Lane13 Rx- | 35 | GND |
| 38 | GND | 37 | Lane6 Tx+ | 38 | GND | 37 | Lane14 Tx+ |
| 40 | Lane6 Rx+ | 39 | Lane6 Tx- | 40 | Lane14 Rx+ | 39 | Lane14Tx- |
| 42 | Lane6 Rx- | 41 | GND | 42 | Lane14 Rx- | 41 | GND |
| 44 | GND | 43 | Lane7 Tx+ | 44 | GND | 43 | Lane15 Tx+ |
| 46 | Lane7 Rx+ | 45 | Lane7 Tx- | 46 | Lane15 Rx+ | 45 | Lane15 Tx- |
| 48 | Lane7Rx- | 47 | GND | 48 | Lane15Rx- | 47 | GND |

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