

## Fact Sheet

MPC852T

POWERQUICC™  
INTEGRATED  
COMMUNICATIONS  
PROCESSOR



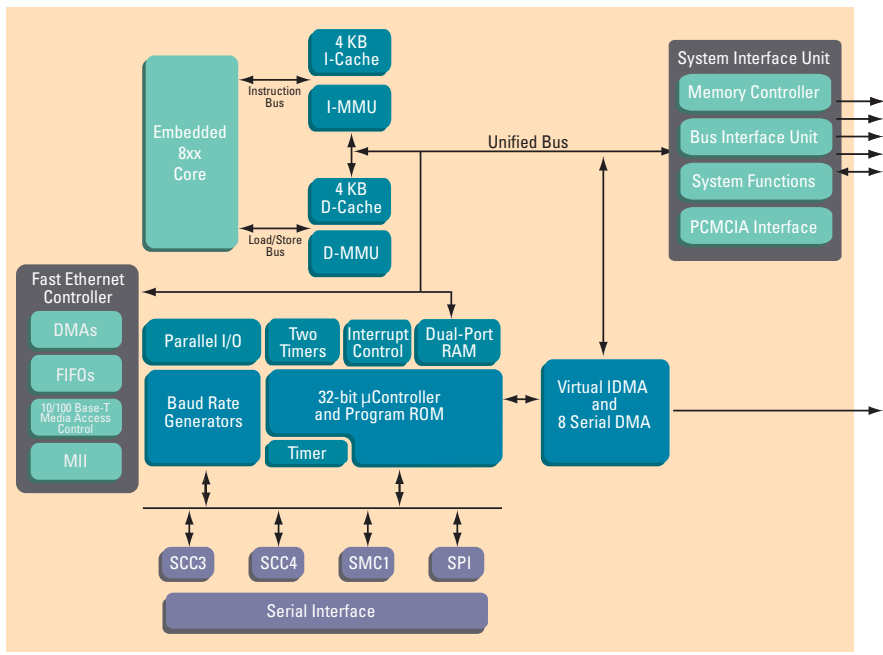
A new member of the PowerQUICC Family, the MPC852T is designed to deliver a versatile, one-chip integrated processor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. Motorola's leading PowerQUICC architecture integrates two processing blocks. One block is an embedded PowerPC™ core and the second block is the communications processor module (CPM). The CPM is designed to support two serial communications controllers (SCCs), providing a total of four serial channels: two SCCs, one serial management controller (SMC) and one serial peripheral interface (SPI). This dual-processor architecture is designed to provide lower power consumption than traditional architectures because the CPM offloads peripheral tasks from the embedded 8xx core.

### PRODUCT HIGHLIGHTS

- Embedded 8xx core
- 4 KB instruction cache
- 4 KB data cache
- Powerful memory controller and system functions
- Efficient architecture that involves a separate RISC processor for handling communications
- PCMCIA interface for 802.11x connectivity
- Up to two serial communications controllers (SCCs)
- Support for Ethernet, Fast Ethernet, HDLC
- One SMC and one SPI
- Many other features—timers, baud rate generators, etc.
- 8K dual-port RAM
- Available in a 256-pin PBGA package
- Strong third-party tools support through Motorola's Smart Networks Alliance Program
- 0.18μ technology
- 1.8V core, 3.3V I/O

Freescale Semiconductor, Inc.

MPC852T



For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)

# Freescale Semiconductor, Inc.

## TYPICAL APPLICATIONS

- Ethernet routers
- Low-end routers
- Line cards
- Wireless LAN
- LAN switches

## TECHNICAL SPECIFICATIONS

- Embedded 8xx microprocessor core providing 132 MIPS (using Dhrystone 2.1) at 100 MHz
  - Single-issue, 32-bit version of the embedded 8xx core with 32-x32-bit fixed point registers
  - 4 KB instruction cache and 4 KB data cache
  - Memory management units with 32-entry TLBs and fully associative instruction and data TLBs
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8-, 16- and 32-bit buses
- Communications Processor Module
  - 8 KB dual-port RAM
  - Up to two serial communications controllers (SCCs)
  - 32-bit scalar RISC controller
  - One serial management controller for UART
  - Eight serial DMA (SDMA) channels
  - One serial peripheral interface
  - Two general-purpose timers
  - Interrupts
  - Two baud rate generators
  - Protocols supported
    - Ethernet IEEE 802.3 and Fast Ethernet
    - HDLC/SDLC
    - UART
    - IrDA
  - Totally transparent mode with/without CRC
- System integration unit
  - Memory controller
  - PCMCIA interface
  - System functions

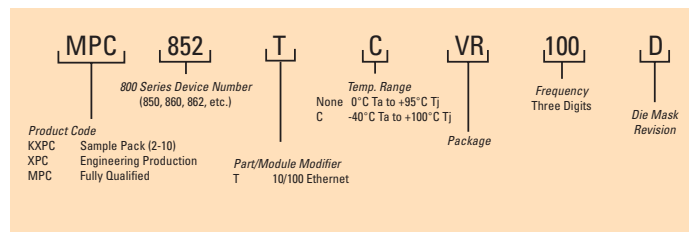
## CONTACT INFORMATION

Motorola offers user's manuals, application notes and sample code for all of its communications processors. Local support for these products is also provided.

This information can be found at: [www.motorola.com/smartnetworks](http://www.motorola.com/smartnetworks).

For all other inquiries, contact the Customer Response Center at

(800) 521-6274 or [www.motorola.com/semiconductors](http://www.motorola.com/semiconductors).



	852T	859DSL	859T	866T	866P
<b>Serial Communications Controllers (SCCs)</b>	2	1	1	4	4
<b>I-Cache (KB)</b>	4	4	4	4	16
<b>D-Cache (KB)</b>	4	4	4	4	8
<b>Ethernet (10T)</b>	Up to 2	1	1	Up to 4	Up to 4
<b>Ethernet (10/100)</b>	Yes	Yes	Yes	Yes	Yes
<b>ATM</b>	No	Yes	Yes	Yes	Yes
<b>Multichannel HDLC</b>	-	-	Up to 32	Up to 64	Up to 64



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