RapidChip™ Semiconductor Platform

OVERVIEW

LSI Logic's RapidChip Semiconductor Platform redefines the custom logic market by offering designers a new alternative to the existing design options of standard-cell ASICs, FPGAs, and ASSPs. RapidChip was developed using LSI Logic's years of experience in ASIC design methodology and manufacturing. The RapidChip platform offers a unique blend of performance and flexibility, while dramatically reducing the design and manufacturing timescales associated with high-performance custom design.

Families of slices aimed at particular applications are provided as the platforms for custom design. The slices contain pre-diffused memory and high-performance system building blocks from LSI Logics's CoreWare® library, along with customizable logic. Additional application-specific CoreWare elements are also provided for mapping into the slices. Customization is accomplished by mapping this CoreWare IP along with the designers' logic to the slice using the metal layers.

Because design implementation is accomplished using the metal layers, tooling costs are kept to an absolute minimum, making high-performance, high-density, deep sub-micron technology and leading-edge IP at affordable. Customers also benefit from dramatically lower production prices when compared to FPGAs, and shorter design and production lead times when compared to standard-cell ASICs.

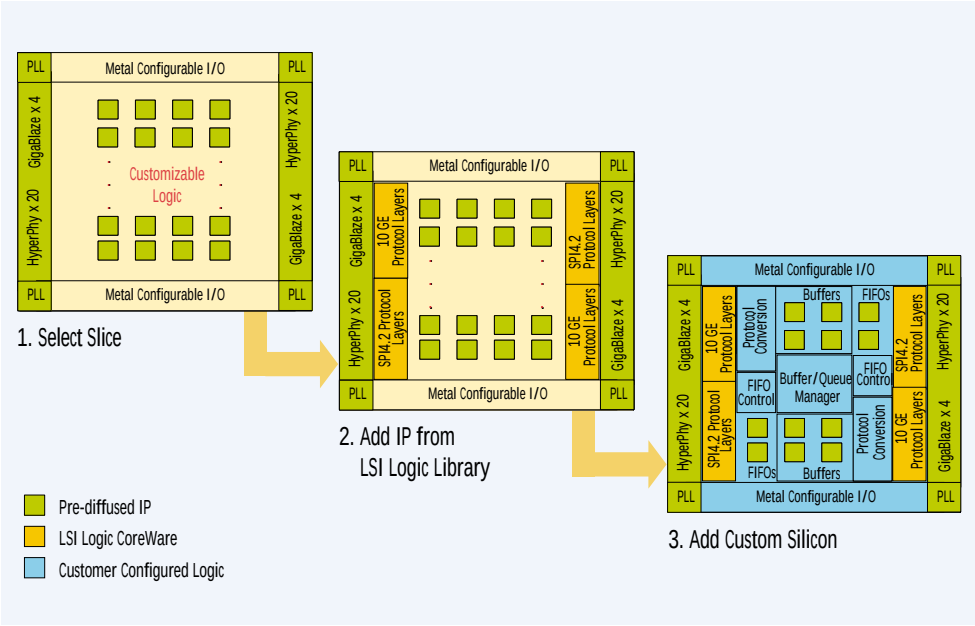

Figure 1: A Communications Example: Three steps to Custom Silicon

FEATURES

- Deep Sub-Micron Technology Platforms
  - Families of slices
  - Embedded Diffused IP
  - Up to 8M Usable Gates
  - Up to 10Mbit Diffused RAM
  - Metal Configurable I/O
  - Offered in 0.18 micron and 0.11 micron
- Tools and Methodology
  - Optimized for Time-To-Market
  - Predictable, Single-Pass Design Closure
  - Slice Specific Verification Environment including Transactors and Monitors
- Generation Tools
  - Memories
  - I/Os
  - Clock Factories
- Pre-diffused Proven CoreWare IP
  - HyperPHY®: 0.6 to 3.2 Gb/s SPI4.2, SPI5 PHY
  - GigaBlaze®: 1 to 4.25 Gb/s Gbit Ethernet, XAUI FibreChannel, Serial ATA Infiniband, PCI Express, RapidIO USB 2.0
  - Processors: ARM®, MIPS® and ZSP™

LSI LOGIC

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- Advanced Proven CoreWare IP
  - SPI4.2, SPI5
  - XGXS
  - Microprocessor Core
  - DDR, RLDRAM Controllers
  - Ethernet MAC 10/100/1G/10G
  - FibreChannel and SCSI Controllers
  - USB host and function
  - PCI/PCIX Controllers
- Memories
  - High Density Single/Multi-Port SRAM
  - Register files
  - High Density CAM
  - ROM

DESIGN FLOW AND PRODUCTIVITY

The time-to-market promise of RapidChip is delivered through the unique advantages of a new design methodology and tool set. This methodology relies on three key elements to provide its accelerated and deterministic flow - a set of automated tools and shells, strict design rules and guidelines, and the inherent predictability of designing with a customizable logic structure. By eliminating lengthy timing closure loops, the RapidChip methodology boosts productivity and enables fast, deterministic throughput from final netlist to prototypes.

A number of views or shells of the selected slice and additional IP are provided to accelerate every phase of the design process. Shells are provided for RTL design, Verification, Static Timing Analysis, Synthesis and Test. As an example, a designer's custom logic is connected to well-defined interfaces within the RTL Shell for the particular RapidChip slice being used, resulting in a simple integration process. Designers also benefit from consistent hierarchy management inherent to the RTL design capabilities within RapidChip methodology.

The verification shell provides an advanced starting point for the functional verification phase of designing a custom device. This ready-made environment includes reference models for all cores, transactors, monitors and protocol checkers.

Shells provide an advanced starting point for the development of static timing analysis scripts in order to accelerate the timing verification phase of the design process. Timing budget management is also enhanced with dedicated on-chip clock factories, automating the generation of complex, multi-domain clocking systems.

LOGIC INTEGRATION

With RapidChip, designers have access to the latest deep sub-micron process technologies without the compromises of Programmable Logic Devices. RapidChip's customizable metal architecture allows for the implementation of up to eight million usable logic gates.

Memory requirements are realized with high-density, pre-diffused cells or by utilizing portions of the customizable logic. Automated tools make implementation choice transparent to the user. Other dedicated tools for generating clock networks, bus structures and test logic -- automate error prone tasks ensuring critical functions are created correct-by-construction.

DELIVERING ON THE PROMISE OF DESIGN RE-USE

RapidChip makes advanced CoreWare IP blocks from LSI Logic available in three forms: hard, soft, and firm.

Hard Cores - High speed transceivers such as HyperPHY® and GigaBlaze®, and CPUs -- are pre-placed using silicon-optimized technology.

Soft Cores - Provided as synthesizeable RTL, implemented in the customizable logic region.

Firm Cores - Implemented in the customizable logic region, relocatable with fixed timing.

I/O cells with metal configurable Vdd and driver characteristics simplify the design process.

BENEFIT

- Combines the best features of Standard Cell ASIC and FPGA:
  - High Performance
  - High Density
  - Low Development Cost
  - Rich IP Coreware Library
  - Fast Time-to-Marktet
  - Reduced Risk
  - Increased Predictability
  - Customizable Benefits

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APPLICATION OPTIMIZED PLATFORMS

With three families of platforms initially available, system designers will find a solution to match their requirements.

	Applications	CoreWare (Firm / Soft IP)		Slice Features (Hard IP)
Communication Platforms	Ethernet Switch Protocol Conversion Backplane Bridge Network Line Card Classifier Traffic Manager	SPI4.2 SPI5 10/100 MAC Gb MAC 10G MAC XGXS	HyperTransport RapidIO MIPS ARM9 DDR RLDRAM	3 - 8 M usable gates 3-10 Mb diffused RAM ARM9, MIPS Ethernet PHY HyperPhy: 622 - 3125 Mb/s GigaBlaze: 1 - 4.25 Gb/s
Storage Platforms	SAN Protocol Conversion Backplane Bridge Tape Drive Host Adapter Board	FiberChannel SCSI CtIr iSCSI Link Layer S-ATA SAS Enet MAC	XGXS ARM7/9 DDR PCI Express Infiniband	3 - 8 M usable gates 3-10 Mb diffused RAM ARM9, MIPS HyperPhy: 622 - 3125 Mb/s GigaBlaze: 1 - 4.25 Gb/s
Consumer Platforms	Home Gateway Set Top Box Cable Headend VoIP Printer	ARM7/9 ZSP USB Link Layer 1394 Link Layer 802.11 Enet MAC	DDR MPEG JPEG PCI PCI-X	3 - 8 M usable gates 3-10 Mb diffused RAM ARM9, MIPS, ZSP PHY: Ethernet, USB HyperPhy: 622 - 3125 Mb/s GigaBlaze: 1 - 4.25 Gb/s

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