リスト3　MacroData，MicroDataを用いた軌道補完のVerilog HDL記述

```
always@(posedge iCLK or posedge iRST)begin

 if(iRST)begin
  rMacroData <= 64'h0000_0000;
  rMicroAddr <= 8'h00;
  rMicroData <= 32'h0000;
  rPWMDATA <= 64'h7f7f_7f7f_7f7f_7f7f;
  rMicroCount <= 3'h0;

  rStart_MTC <= 0;
  rStart_keisan <= 0;
  rStart_PG <= 0;

  rFIN <= 0;

  rState <= ps0;
 end

 else begin
  case(rState)

   ps0:begin //Start & Wait
    //rMacroData <= iMacroData;
    //rMicroAddr <= iMicroAddr;
    rMicroData <= rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= 0;
    rStart_PG <= 0;

    rFIN <= 0;

    if(iSTART)begin
     rMacroData <= iMacroData;
     rMicroAddr <= iMicroAddr;
     rState <= ps1;
    end
    else begin
     rMacroData <= rMacroData;
     rMicroAddr <= rMicroAddr;
     rState <= ps0;
    end
   end

   ps1:begin //Get MacroData & Start MTC
    rMacroData <= rMacroData;
    rMicroAddr <= rMicroAddr;

    rMicroData <= rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= rMicroCount;

    rStart_MTC <= 1;
    rStart_keisan <= 0;
    rStart_PG <= 0;

    rFIN <= 0;

    rState <= ps2;
   end

   ps2:begin //Get MicroData;
    rMacroData <= rMacroData;
    rMicroAddr <= rMicroAddr;

    rMicroData <= iFIN_MTC ? iMicroData : rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= iFIN_MTC ? 1: 0;
    rStart_PG <= 0;

    rFIN <= 0;

    rState <= iFIN_MTC ? ps3: ps2;
   end

   ps3:begin //SetPWMDATA
    rMacroData <= rMacroData;
    rMicroAddr <= rMicroAddr;

    rMicroData <= rMicroData;

    if(rMicroCount >= 7)begin
     rPWMDATA <= wFIN_K ? rMacroData : rPWMDATA;
    end
    else begin
     rPWMDATA <= wFIN_K ? wPWMDATA_Keisan : rPWMDATA;
    end

    rMicroCount <= rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= 0;
    rStart_PG <= 0;

    rFIN <= 0;

    rState <= wFIN_K ? ps4: ps3;
   end

   ps4:begin //Start PulseGene & SetNextAddr
    rMacroData <= rMacroData;
    rMicroAddr <= rMicroAddr;

    rMicroData <= rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= 0;
    rStart_PG <= 1;

    rFIN <= 0;

    rState <= ps5;
   end

   ps5:begin
    rMacroData <= rMacroData;
    rMicroAddr <= iFIN_PG ? rMicroAddr+1 : rMicroAddr;

    rMicroData <= rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= iFIN_PG ? rMicroCount+1 : rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= 0;
    rStart_PG <= 0;

    rFIN <= 0;

    rState <= iFIN_PG ? ps6: ps5;
   end

   ps6:begin
    rMacroData <= rMacroData;
    rMicroAddr <= rMicroAddr;

    rMicroData <= rMicroData;
    rPWMDATA <= rPWMDATA;
    rMicroCount <= rMicroCount;

    rStart_MTC <= 0;
    rStart_keisan <= 0;
    rStart_PG <= 0;

    if(rMicroCount == 0)begin
     rState <= ps0;
     rFIN <= 1;
    end
    else begin
     rState <= iFIN_PG ? ps6: ps1;
     rFIN <= 0;
    end
   end
  endcase
 end
endmodule
```